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36491/PBH/B600 (BP 1093)

CLAIMS

1. An integrated circuit inductor comprising:
a substrate; and
a spiral inductor metalization pattern disposed on the substrate including a plurality of parallel tracks in a spiral patern each track having a first end and a second end and having the first ends coupled together and the second ends coupled together.

2. The integrated circuit inductor of claim 1, wherein the substrate is fabricated utilizing a CMOS process.

3. The integrated circuit inductor of claim 1, wherein the spiral inductor is a square configuration.

4. The integrated circuit inductor of claim 1, wherein the spiral inductor is a octagonal configuration.

5. The integrated circuit inductor of claim 1, in which the multiple tracks are disposed in a common layer.

6. The integrated circuit inductor of claim 1, in which the multiple tracks are disposed in different layers.

7. The integrated circuit inductor of claim 1, in which the multiple tracks are disposed in different layers and coupled with a via.

8. The integrated circuit inductor of claim 1, further comprising a shield disposed in a layer beneath the integrated circuit inductor.

9. The integrated circuit inductor of claim 8, in which the shield is disposed by an n+ diffusion.

10. The integrated circuit inductor of claim 8, in which the shield is formed in a fingered pattern from n+ material having fingers electrically isolated by regions of polysilicon.

11. The integrated circuit inductor of claim 8, in which the fingered pattern is coupled to a common ground reference.

12. The integrated circuit inductor of claim 8, in which the shield further comprises a second fingered pattern coupled to the common ground reference by a conductive strip that does not provide a ground loop path.

13. An integrated circuit inductor comprising:

a substrate;

a first track disposed on the substrate in a spiral pattern; and

a second track disposed on the substrate in a spiral pattern substantially identical to the first pattern and substantially oriented parallel to the first track.

14. An integrated circuit inductor comprising:

a substrate having a first layer and a second layer;

a first track disposed on the first layer in a first spiral pattern;

a second track disposed on the second layer in a second spiral pattern substantially identical to the first spiral patten and substantially oriented parallel to the first spiral pattern; and

a pattern of via holes sufficient to couple a varying voltage present along the length of the first track on to the second track.

15. An integrated inductance comprising:

a substrate having a first layer and a second layer;

a first outer transmission line disposed on the first layer in a spiral pattern;

a second inner transmission line disposed on the first layer in a spiral pattern such that the second inner transmission line is loosely coupled to the first outer transmission line, and having a first transmission line first end directly coupled to a second transmission line first end and a first transmission line second end directly coupled to a second transmission line second end;

a third outer transmission line disposed on the second layer in a spiral pattern and aligned substantially directly above the first transmission line and directly coupled to the first transmission line; and

a fourth inner transmission line disposed on the substrate's second layer in a spiral pattern such that the fourth inner transmission line is coupled to the first transmission line and aligned substantially directly above the second transmission line and directly coupled to the second transmission line.

16. An integrated circuit inductor comprising:

a substrate means for constructing an integrated circuit;

a first means for producing an inductance disposed on the substrate having a length;

a second means for producing an inductance disposed on the substrate having a length; and

a coupling means for establishing a common potential between the first and second means for producing an inductance at substantially the same position along the length of the first and second means for producing an inductance.

17. A method for producing an integrated circuit inductor comprising:

disposing a first multi-track spiral having a plurality of tracks upon a first semiconductor substrate layer;

disposing a second multi-track spiral having a plurality of tracks upon a second semiconductor substrate in vertical alignment to the first spiral;

connecting the ends of the tracks including the first multi-track spiral at one end;

coupling the first multi-track spiral having a plurality of tracks to the second multi-track spiral having a plurality of tracks with a via;

coupling the tracks at a first end of the first multi-track spiral having a plurality of tracks to the tracks at a first end of the second multi-track spiral having a plurality of tracks; and

coupling the tracks at a second end of the first multi-track spiral having a plurality of tracks to the tracks at a second end of the second multi-track spiral having a plurality of tracks.

18. The method for producing an integrated circuit inductor of claim 17, in which the shield further comprises:

a first fingered pattern constructed from a n+ diffusion layer;

a second fingered pattern inter-digitated with the first and constructed of a poly-silicon material; and

a coupling structure coupling the fingers of the first finger pattern to a ground reference.

19. The method for producing an integrated circuit inductor of claim 17, wherein the shield further comprises:

a third fingered pattern including a n+ diffusion layer

a fourth fingered pattern inter-digitated with the third and including a poly-silicon material;

a coupling structure coupling the fingers of the first finger pattern to a ground reference; and

a coupling structure coupling the fingers of the third finger pattern to a ground reference.

20. The method for producing an integrated circuit inductor of claim 17, in which the coupling structure further comprises a break in the structure.

21. An integrated filter comprising

a substrate;

a switched capacitor disposed on the substrate; and

an integrated circuit inductor disposed on the substrate and coupled to the capacitor to provide a filter structure.

22. A method of increasing inductor Q in a semiconductor device, comprising the steps of:

providing one or more semiconductor substrate layers; and

layering a first plurality of spiral inductor conductive paths on a first one of said semiconductor substrate layers, each of the first plurality of spiral inductor conductive paths running parallel with each other and having a gap therebetween, and each of the first plurality of spiral inductor conductive paths having a proximal end and a distal

end, the proximal end of each of the first plurality of spiral inductor conductive paths being interconnected and the distal end of each of the first plurality of spiral inductor conductive paths being interconnected.

23. The method of increasing inductor Q in a semiconductor device of Claim 1, further comprising the step of:
layering at least a one or more second spiral inductor conductive paths on a second one of said semiconductor substrate layers, said one or more of said second spiral inductor conductive paths running parallel to and being via connected to a corresponding one of said first plurality of spiral inductor conductive paths.